

ABSTRACT

A two stage amplifier circuit (10), the first stage (12) comprising a modified quad configuration and the second stage (14) comprising a translinear current
5 amplifier configuration. The present invention achieves the advantages of fast response time, low distortion and improved bandwidth. The current gain of the second stage is represented by:

$$(IA_{out1} - IA_{out2}) / (I_{out1} - I_{out2}) = (1 + R_{123} / R_{124}) \cdot (I_{135} / I_{134}) \cdot (A / (1 + A))$$

10 where $A = g_{m Q109} \cdot R_{124}$.